

DN9002K10PCIE8T Errata

Last Update: October 8, 2007

1) Differential Polarity On Daughtercards

Symptom/Problem

The signal DCA1N29 connects to “P” pin on the FPGA, and the signals DCA1P29 connects to “N” pin on the FPGA.

Impact

Only customers who are using one of these three pairs as a differential signal are affected. Single-ended use of these signals is not impacted.

Solution/Work-Around

When using daughtercards requiring differential signaling on these pins, then the FPGA RTL must invert the transmitted or received logic. The differential input buffer should connect so that the .I connects to a “P” pin on the FPGA, and the .IB port connects to an “N” pin on the FPGA.