

# DN9200K10PCI Errata

Last Update: June 20, 2008

## 1) Differential Polarity On Daughtercards

### **Symptom/Problem**

The signal DCA1N29 connects to “P” pin on the FPGA, and the signals DCA1P29 connects to “N” pin on the FPGA. **Impact** Only customers who are using one of these three pairs as a differential signal are affected. Single-ended use of these signals is not impacted.

### **Solution/Work-Around**

When using daughtercards requiring differential signaling on these pins, then the FPGA RTL must invert the transmitted or received logic. The differential input buffer should connect so that the .I connects to a “P” pin on the FPGA, and the .IB port connects to an “N” pin on the FPGA.

## 2) Ethernet RXCLK

### **Symptom/Problem**

When the Ethernet RXCLK signal is connected to a BUFR, the place-and-route tool cannot finish.

### **Solution/Work-Around**

The placement of the BUFR can be done manually, using this line in the UCF:

```
INST “xxxx” LOC = “BUFRX0Y4”
```

Where xxxx is the RTL path to the BUFR instantiation.

